IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

Application No.: 09/696,826)
)
Applicant: CHOW, Lap-Wai et al.) Examiner: Thien Tran
) Group Art Unit 2811
Filed: October 25, 2000)
) Our Ref: B-3650
For: "Implanted Hidden Interconnections...") (617089-5/RPB)

Re: **RULE 132 DECLARATION**

DECLARATION UNDER 37 C.F.R. § 1.132

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

I, Lap-Wai Chow, Declare and say:

1. I am one of the co-inventors in the above-identified application.
2. I graduated with a Masters. in electrical engineering from the Chinese University of Hong Kong, in 1980.
3. I have been working in the field of semiconductor technology for 22 years.
4. I have read and I am familiar with the above-identified application, and I have read U.S. Patent No. 6,215,158 (the Choi patent). I have also read the Office Actions of February 19, 2002 and August 27, 2002. I have also read the Advisory Action of November 18, 2002.
5. I submit that Choi does not teach, disclose, or suggest the invention as described and claimed in the present application. Further, I submit that Choi in combination with the knowledge of one skilled in the art does not teach, disclose or suggest the invention as claimed in the present application.
6. The above-identified patent application describes, among other things, a camouflaged interconnection scheme for interconnecting two spaced-apart

first conductivity type implanted regions. The camouflaged interconnection scheme has a first conductivity type implanted region forming a conducting channel between the two spaced-apart first conductivity type implanted regions. Further, the camouflaged interconnection scheme has a second implanted region of a second conductivity type overlying the conducting channel. The camouflaged interconnection scheme is claimed, for example, in independent claims 1, 5, 15, 18 and 19.

7. Choi does not disclose a camouflaged interconnection scheme.

8. In the Office Action of February 19, 2002, the Examiner asserts that " Choi discloses the same interconnection structure as claimed ...As a result, what is true in present invention is also true in the Choi reference. The second dope[d] region 121 of Choi inherently camouflages the buried interconnect 130 and inhibits reverse engineering. This is not correct. Choi teaches in col. 3, lines 37-42 " The dielectric 190 has been patterned with openings 240, 250 to expose a portion of the first and second source regions 140, 150 respectively. A high energy beam of n-dopant may now be used to create implanted plugs 231, 232 thereby forming connections between the interconnect layer 130 and the first and second source regions 140, 150." In col. 3, lines 54-55, Choi teaches " Conductive plugs 440, 450, 460 are deposited using conventional techniques to fill the openings 240, 250, 360, respectively." Choi further teaches in col. 3, lines 58-67 that " Conductive plug 460 will ultimately provide a conventional contact for drain region 160. However, conductive plugs 440, 450 are dummy plugs, which are not to be used for contacting other parts of the semiconductor, but rather are simply used to fill the openings 240, 250 remaining after the formation of the implanted plugs 231, 232. Further connection of the first and second source regions 140, 150 to other parts of the semiconductor will be accomplished by connecting the interconnect layer 130 through a connection not shown."

9. Thus, Choi teaches that the conductive plugs 440, 450, 460 are present only for two purposes. One purpose, which is served by conductive plug 460, is to provide a conventional contact. The second purpose, which is served by conductive plugs 440, 450, is to provide a contact to the underlying interconnect layer 130. Thus, a reverse engineer will see the conductive plugs 440, 450 which are not used for contacting other parts of the semiconductor and would immediately infer that a connection has been made via the interconnect layer 130. Therefore, the interconnection scheme of Choi is not camouflaged at all.

10. In response to the argument given in 8 and 9 above, the Examiner asserts in the Advisory Action of November 18, 2002, that the reverse engineer would not know how and which source/drain regions were connected to each other by the interconnect layer 130 because not all source/drain regions in the device are connected to each other. This is incorrect. First, a reverse engineer when looking at a plan view (top down) of a structure according to Choi would see metal plugs. Some metal plugs would be connected to metal lines (herein referred to as dummy plugs) and some metal plugs would not be connected. In standard circuit manufacturing, metal plugs are only used to provide a connection. If a source/drain is not to be connected it will not have a metal plug associated with it. Thus, the reverse engineer will immediately know by the presence of the dummy plugs that something else must be going on. Then, the reverse engineer would take a cross section of just one of the dummy plugs and see the connection to the interconnect layer. Because each dummy plug indicates a connection to the interconnect layer. The reverse engineer would now know the location of the interconnections.

11. In contrast, a reverse engineer when looking at the invention as described and claimed would not see any indication that there were any connections other than the connections indicated by the metal lines. Even if the reverse engineer were to cross section one of the source/drain regions, it is unlikely

that the reverse engineer would pick the region that was connected to another region through a buried interconnect. Further, even if the reverse engineer was fortunate enough to discover the presence of the buried interconnect, there is no hint from the top down view which regions are connected with a buried interconnect and which regions are not. Thus, the reverse engineer would have to effectively cross section the device at each implant to discover the location of each interconnection. Forcing the reverse engineer to cross-section each active region would force many reverse engineers to give up or spend considerable time and resources.

12. The present invention as described and claimed, provides an important capability not provided in the apparatus disclosed by Choi. The present invention provides the capability to camouflage the connections between two spaced apart regions. The camouflage of the connections makes the reverse engineering of the circuit very difficult. Further, there is no hint when looking at the circuit from plan view (top down) that the circuit has been modified in any way.

13. I declare further that all statements made herein of my own knowledge are true; that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patents issuing thereon.

Date: Dec. 20th, 2002

Lap-Wai Chow

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PATENT

Application No.: 09/696,826)
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Applicant: CLARK, William, et al.) Examiner: Thien Tran
) Group Art Unit 2811
Filed: October 25, 2000)
) Our Ref: B-3650
For: "Implanted Hidden Interconnections...") (617089-5/RPB)

#17 Declaration FJONES 1-21-03

Re: **RULE 132 DECLARATION**

DECLARATION UNDER 37 C.F.R. § 1.132

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

I, William M. Clark, Jr., Declare and say:

1. I am one of the co-inventors in the above-identified application.
2. I graduated with a Ph.D. in electrical engineering from the University of California, Berkeley, in 1968.
3. I have been working in the field of semiconductor technology for 22 years.
4. I have read and I am familiar with the above-identified application, and I have read U.S. Patent No. 6,215,158 (the Choi patent). I have also read the Office Actions of February 19, 2002 and August 27, 2002. I have also read the Advisory Action of November 18, 2002.
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Date: 19 Dec 02

William M. Clark, Jr.